# UM10079

## ISP1504A1; ISP1504C1 ULPI transceiver evaluation board, supporting Hi-Speed USB host, peripheral and OTG

**Rev. 01 — 3 December 2007** **User manual**

### Document information

| Info | Content |
|---|---|
| **Keywords** | isp1504x1, usb, ulpi, universal serial bus, transceiver, utmi+ low-pin interface, host, peripheral, otg, usb 2.0, phy |
| **Abstract** | The document describes how the ISP1504x1 eval board can be configured to interface with link to provide a USB physical layer front-end solution. This document also includes the schematic of the eval board and the components needed to integrate the ISP1504x1 to the user's system. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 01 | 20071203 | First release. |

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# 1. Introduction

The ISP1504A1; ISP1504C1 (ISP1504x1) is an 8-bit bidirectional UTMI+ Low Pin Interface (ULPI) transceiver, which provides a Hi-Speed Universal Serial Bus (USB) analog front-end solution to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) to implement as a Hi-Speed USB host, peripheral or OTG device.

The ISP1504x1 evaluation (eval) board allows designers to evaluate the features of the ISP1504x1, and conduct system-level validation and testing. The eval board interfaces to the link through a 100-pin Transceiver and Macrocell Tester (T&MT) connector that complies with *USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2*.

Fig 1 shows the ISP1504x1 eval board.

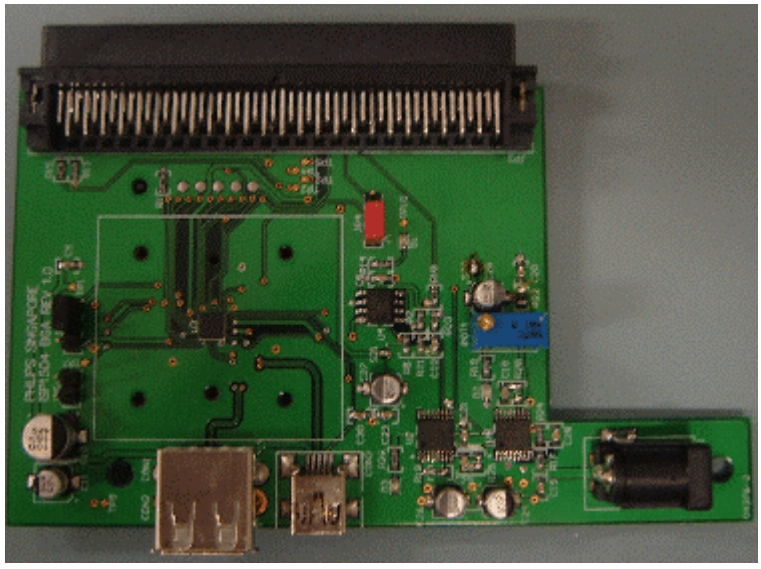

**Fig 1. ISP1504x1 eval board**

# 2. Board features

## 2.1 Functionality

- The ISP1504x1 is fully compliant with *Universal Serial Bus Specification Rev. 2.0, UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3.*
- The T&MT connector interface is fully compliant with *USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2.*
- The $V_{BUS}$ power must be supplied by the on-board power switch.
- Adjustable $V_{CC}$ voltage when powered by the 5 V DC power supply.
- Flexible clock source for the ISP1504x1: on-board crystal or square wave clock driven into the XTAL1 input.

### 2.2 Connectors

- USB connectors: standard-A (mounted by default), standard-B and mini-AB (mounted by default)
- T&MT connector to interface to the link
- Input power connector

### 2.3 Power supplies

- Supplied by the 5 V DC power supply through the input power connector, or
- Supplied by the link through the T&MT connector

## 3. Board usage

### 3.1 Overview

The ISP1504x1 eval board is designed to connect to a link board through the T&MT connector for system validation as shown in Fig 2.

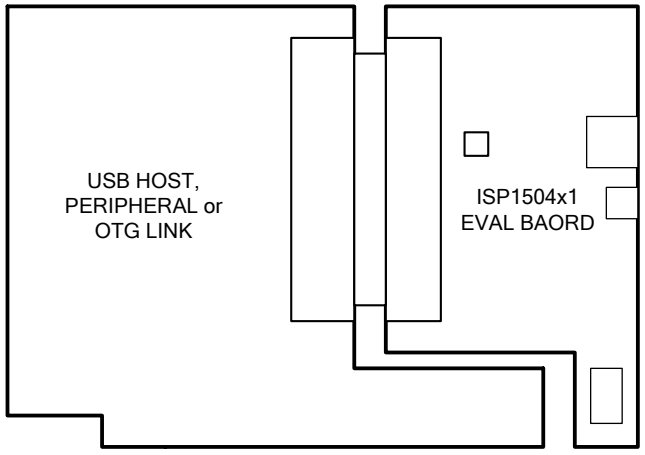


**Fig 2. ISP1504x1 eval board connected to the link board**

### 3.2 Block diagram

Fig 3 shows the high-level block diagram of the ISP1504x1 eval board.

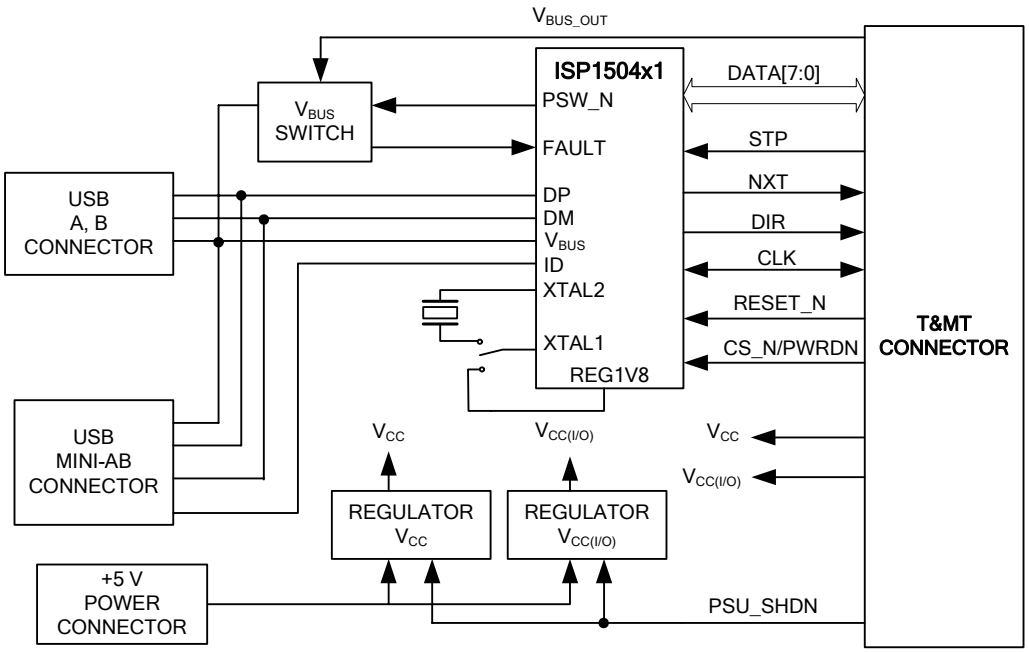


**Fig 3. ISP1504x1 eval board block diagram**

## 3.3 Power supply

The ISP1504x1 eval board can be powered either from the input power connector (SW1) or from the T&MT connector (JP3). When power is supplied from the link through the T&MT connector, pin 100 of the connector must be connected to ground on the link side. This will shut down $V_{CC}$ and $V_{CC(I/O)}$ regulator outputs to the ISP1504x1. When power is supplied from the input power connector, pin 100 of the T&MT connector must be left open on the link side.

There are two regulators on the eval board supplying $V_{CC}$ and $V_{CC(I/O)}$. Regulator U6 supplying $V_{CC}$ has an adjustable output voltage, which must be set to a voltage between 3.0 V and 4.5 V by tuning POT1. Regulator U7 supplying $V_{CC(I/O)}$ has a fixed output voltage of 3.3 V. Solder bridges S20 and S21 must always be closed. LED D2 indicates the existence of $V_{CC}$.

## 3.4 $V_{BUS}$ power switch

For host or OTG applications, an external power switch is required to supply 5 V to $V_{BUS}$. *Universal Serial Bus Specification Rev. 2.0* allows continuous shorting between $V_{BUS}$ and ground. Therefore, the power switch is required to detect overcurrent condition and thermally shut down. So, an external active-LOW enabled power switch with digital fault output, for example, MIC2026-2, is required. On the eval board, an external power switch (U4) with digital fault output is implemented.

The link must supply 5 V to the power switch through pin 28 of the T&MT connector.

Table 1 lists the register bits that must be configured to utilize the external power switch. When the DRV_VBUS_EXT register bit is set, the ISP1504x1 will output LOW on PSW_N to turn on the power switch. Once the $V_{BUS}$ power switch is turned on, green LED D1 will light up.

**Table 1. Register bits related to the external $V_{BUS}$ power switch**

| Register | Remark |
|---|---|
| DRV_VBUS_EXT | Set to turn on the external $V_{BUS}$ power switch<br>Cleared to turn off the external $V_{BUS}$ power switch |
| DRV_VBUS | Cleared (power on default value) |
| USE_EXT_VBUS_IND | Set to detect fault condition output from the external power switch |
| IND_COMPL | Set if the fault output from the power switch is active HIGH.<br>Cleared if it is active LOW |

## 3.5 USB connectors

There are two USB connectors mounted on the eval board by default, standard-A USB connector and mini-AB USB connector. For a peripheral application, the standard-B connector must replace the standard-A USB connector.

The DP and DM lines are switched between the two USB connectors using a 0 Ω link resistor to achieve better signal quality. If the eval board is used for a host or peripheral application, DP and DM of the ISP1504x1 must be routed to the DP and DM pins of the standard-A or standard-B USB connector, respectively. In this case, R4 and R5 must be mounted, and R11 and R12 must be removed (default). If the eval board is used for an OTG application, DP and DM of the ISP1504x1 must be routed to the DP and DM pins of the mini-AB connector, respectively. In this case, R11 and R12 must be mounted, and R4 and R5 must be removed.

For a peripheral or OTG application, the capacitance on $V_{BUS}$ must be limited to be less than 10 µF or 6.5 µF so that there will not be a large in-rush current when connected. Therefore, jumper J5 must be off. For a host application, jumper J5 must be on so that the 100 µF filter capacitor will prevent the voltage on $V_{BUS}$ from dropping below 4.5 V, when a downstream device is connected.

## 3.6 CS_N/PWRDN

The CS_N/PWRDN pin of the ISP1504x1 allows the ULPI interface to be shared with other ICs. Driving the CS_N/PWRDN pin to LOW will 3-state the DATA, NXT and DIR pins. Therefore, other ICs can use these pins.

On the eval board, short pin 1 and pin 2 of JP4 (default) to permanently short CS_N/PWRDN to ground. It can, however, be controlled from the link by shorting pin 2 and pin 3 of JP4. Therefore, the link can select or de-select the ISP1504x1 by driving pin 18 of the T&MT connector to either LOW or HIGH.

When CS_N/PWRDN is configured as HIGH (JP4 open), the ISP1504x1 is in power-down mode.

## 3.7 RESET_N

The reset signal of the ISP1504x1 is an active-LOW asynchronous input that resets all internal circuitry.

The link can control the reset signal of the ISP1504x1 through pin 17 of the T&MT connector.

### 3.8 Clock supply

There are two ways to provide a clock to the ISP1504x1:

- Attach a crystal between XTAL1 and XTAL2. In this case, a jumper must be installed between pin 2 and pin 3 of JP1. The frequency of the crystal is 19.2 MHz.
- Drive an external clock into pin XTAL1. In this case, the jumper on pin 2 and pin 3 of JP1 must be removed and an external clock source must be applied on pin 2 of JP1. The frequency of the external clock is 19.2 MHz.

### 3.9 ESD protection

The ISP1504x1 has an internal ElectroStatic Discharge (ESD) protection diode that can withstand 2 kV for the ID, DP, DM and $V_{BUS}$ pins. Therefore, an external protection diode is not required if 2 kV protection is good enough for the application. U1 or U2 is recommended external protection diode if 15 kV ESD protection is required.

### 3.10 Configuration summary

A summary of the eval board configurations for various applications is given in Table 2.

**Table 2. Summary of the transceiver configuration for various applications**

| Configurable setting | | Host application | Peripheral application | OTG application |
|---|---|---|---|---|
| DP and DM routing | R4 and R5 | Mounted | Mounted | Not mounted |
| | R11 and R12 | Not mounted | Not mounted | Mounted |
| $V_{BUS}$ capacitance | JP5 | Short | Open | Open |
| $V_{CC}$ power | S20 | Short | Short | Short |
| $V_{CC(I/O)}$ power | S21 | Short | Short | Short |
| Clock selection | JP1 | Short pins 1 and 2: input 60 MHz on CLOCK | Short pins 1 and 2: input 60 MHz on CLOCK | Short pins 1 and 2: input 60 MHz on CLOCK |
| | | Short pins 2 and 3: use 19.2 MHz crystal | Short pins 2 and 3: use 19.2 MHz crystal | Short pins 2 and 3: use 19.2 MHz crystal |
| | | Open: use 19.2 MHz CLOCK on pin XTAL1 | Open: use 19.2 MHz CLOCK on pin XTAL1 | Open: use 19.2 MHz CLOCK on pin XTAL1 |
| Chip selection | JP4 | Short pins 1 and 2: chip active | Short pins 1 and 2: chip active | Short pins 1 and 2: chip active |
| | | Short pins 2 and 3: controlled by link | Short pins 2 and 3: controlled by link | Short pins 2 and 3: controlled by link |
| | | Open: chip power-down | Open: chip power-down | Open: chip power-down |

## 4. Quick troubleshooting guide

Following is a step-by-step guide to troubleshoot the ISP1504x1 eval board, if you encounter any problem.

1. Check the printing on the IC package to ensure that you have the latest revision. The last letter on the third line indicates the revision of the chip.

2. Power the eval board through the SW1 connector with a 5 V power supply.
3. Measure the voltage at $V_{CC}$. It must be between 3.0 V and 4.5 V. Measure the voltage at $V_{CC(I/O)}$. It must be around 3.3 V. If both regulators give no output, check whether PSU_SHDN is pulled up to 5 V. If only one regulator gives abnormal output, it is likely that the regulator is faulty.
4. Measure the voltage at the RREF pin of the ISP1504x1. The voltage must be around 1.20 V to 1.27 V. If the voltage at the pin is abnormal, it is likely that the chip is not properly soldered on the PCB or the IC is damaged.
5. Measure the output voltage at REG1V8 and REG3V3. These voltages must be 1.8 V and 3.3 V, respectively. If the voltage at these pins is abnormal, it is likely that the IC is damaged.
6. Ensure that configuration settings are as given in Table 2.
7. Probe the CLOCK pin of the ISP1504x1 with an oscilloscope. A 60 MHz clock must be observed. If there is no output on the CLOCK, check if the chip is selected, that is, a jumper must be installed on pins 1 and 2 of JP4.
8. If the link cannot perform any TXCMD, check whether the RESET_N pin is HIGH during operation.

## 5. PCB guideline

The ISP1504x1 eval board has four layers. The top and bottom layers consist of signal, power tracks and ground fill, while the second and third layers are power and ground planes.

It is recommended that you follow these guidelines when designing a PCB:

- To get stable band gap reference $V_{REF}$, place $R_{RREF}$ resistor R9 close to pin 3 of the ISP1504x1. The 12 kΩ resistor connected to $R_{RREF}$ must have a tight tolerance 1 % or better.
- Place decoupling capacitors close to the supply pins of the ISP1504x1. Each $V_{CC(I/O)}$ pin must be decoupled using one decoupling capacitor. If there is a high-radiated emission, ferrite beads can be used, and must be placed close to supply pins $V_{CC(I/O)}$ and $V_{CC}$. Ferrite beads used in the application can be between 50 Ω and 120 Ω at 100 MHz, with a current rating of approximately 200 mA.
- Place decoupling and filtering capacitors close to the output pins of the 1.8 V and 3.3 V regulators.
- Place the crystal oscillator and two load capacitors close to XTAL1 and XTAL2 of the IC to avoid unstable oscillation because of resonance from parasitic inductance and capacitance.
- To achieve differential impedance of 90 Ω on the DP and DM lines, the trace width and spacing of DP and DM must comply with *Universal Serial Bus Specification Rev. 2.0* requirement of 7.5 mils width and 7.5 mils spacing. Also, the parallelism of the DP and DM lines must be maintained. Avoid stubs on lines.
- Ground vias are recommended for ground plane interconnect and must be kept apart by a maximum distance of 10 mm x 10 mm.
- Route the clock out away from the data line to avoid crosstalk. If the clock signal is distorted by reflection, a series termination resistor can be considered. The termination resistor must be placed closed to the clock source.

# 6. Components required when integrating

Table 3 provides the components that are required when integrating the ISP1504x1 into the system. For more information, refer to the ISP1504x1 data sheet.

**Table 3. Components required when integrating the ISP1504x1**

| Designator | Component description | Location | Value | Remark |
|---|---|---|---|---|
| R9 | Resistor for band gap reference | On RREF | 12 kΩ ± 1 % | - |
| C10, C11 | Filter capacitor | On $V_{BUS}$ | See Table 4 | - |
| C7 | Decoupling capacitor | On REG3V3 | 100 nF ± 10 % | - |
| C13 | Filtering capacitor | On REG3V3 | 4.7 µF ± 10 % | - |
| X1 | Crystal | Between XTAL1 and XTAL2 | 19.2 MHz ± 50 ppm | Recommended crystal specification: Crystal drive level: 500 µW max; ESR ≤ 100 Ω max; shunt package capacitance = 7 pF max. |
| C15, C16 | Crystal load capacitor | Between XTAL1 and ground and XTAL2 and ground | 18 pF ± 10 % | Not required if using clock from another source |
| C6 | Decoupling capacitor | On REG1V8 | 100 nF ± 10 % | - |
| C12 | Filter capacitor | On REG1V8 | 4.7 µF ± 10 % | - |
| C1, C2, C3 | Decoupling capacitor for $V_{CC(I/O)}$ | On each $V_{CC(I/O)}$ pin | 100 nF ± 10 % | - |
| C4 | Decoupling capacitor for $V_{CC}$ | On $V_{CC}$ | 100 nF ± 10 % | - |
| U4 | $V_{BUS}$ power switch | Between FAULT AND PSW_N | $V_{BUS}$ power switch with digital fault output | Required only if driving more than 50 mA on $V_{BUS}$ |
| R7 | Pull-up resistor | On PSW_N | 10 kΩ ± 5 % | Required if $V_{BUS}$ power switch is needed |

**Table 4. Recommended $V_{BUS}$ capacitor**

*These values are according to the Universal Serial Bus Specification Rev. 2.0 and On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3 requirements.*

| $CV_{BUS}$ | Min | Max | Unit |
|---|---|---|---|
| Host | 120 | - | µF |
| OTG | 1 | 6.5 | µF |
| Peripheral | 1 | 10 | µF |

# 7. Schematics

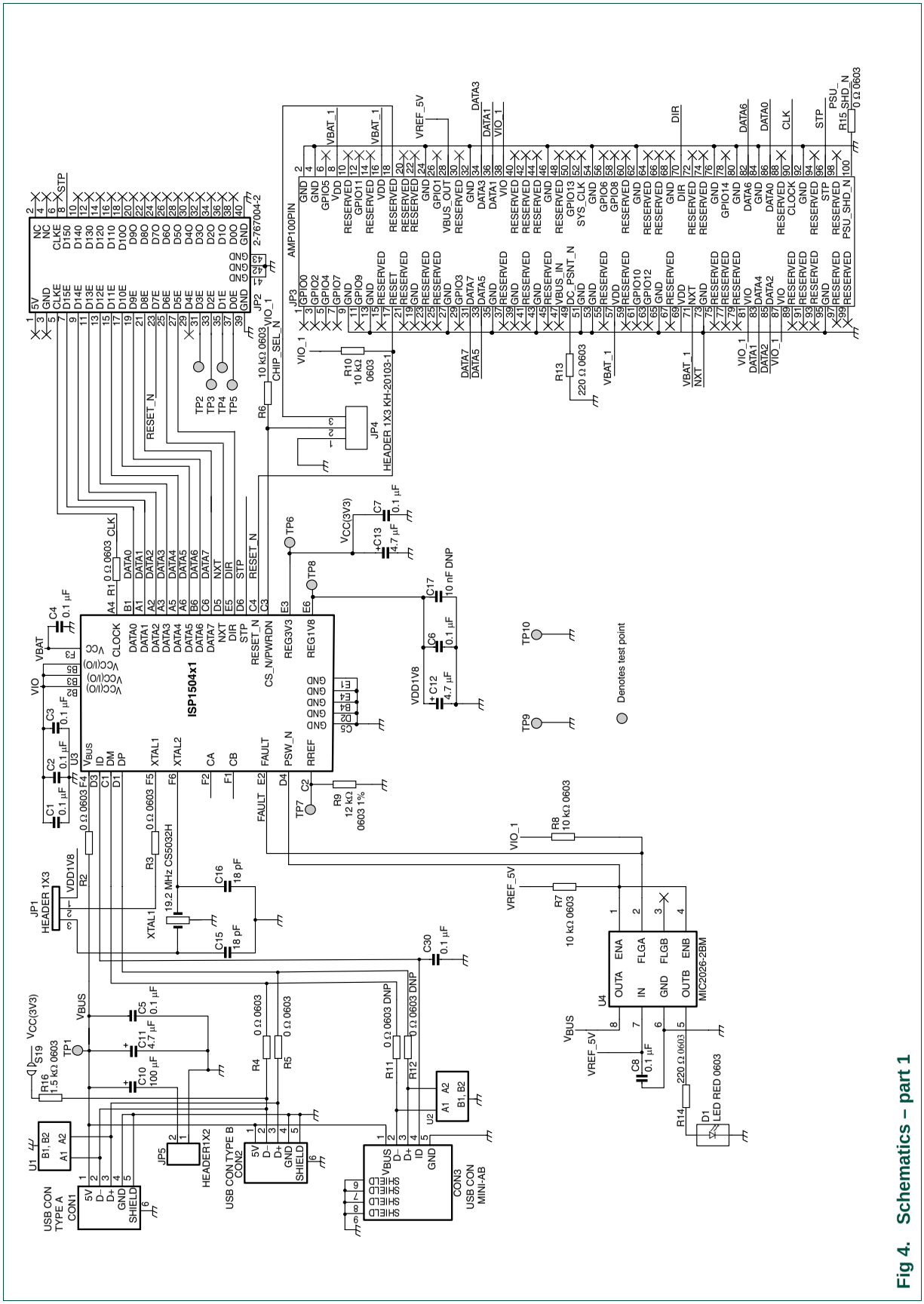


Fig 4. Schematics – part 1

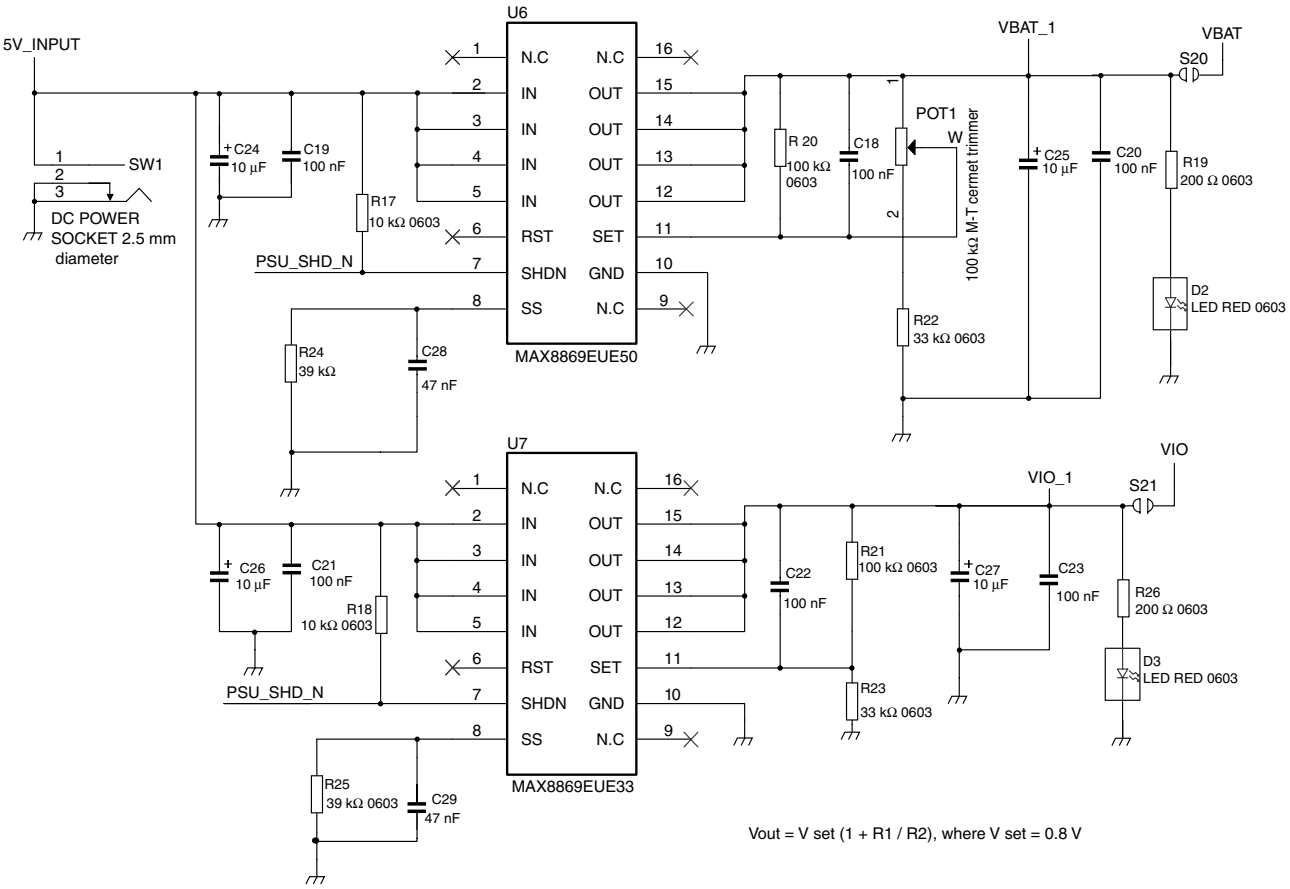


**Fig 5. Schematics – part 2**

# 8. Bill of materials

**Table 5. Bill of materials**

| Designator | Footprint | Comment |
|---|---|---|
| R401, R402, R403, R404, R405, R406, R419 | 0603 | 0 Ω |
| R407, R410, R412, R414, R416, R418 | 0603 | 10 kΩ |
| C408, C410, C412, C414, C416, C418, C421, C423, C424, C425, C426, C427, C402, C406 | 0603 | 100 nF |
| R400 | 0603 | 12 kΩ ± 1 % |
| R409 | 0603 | 18 kΩ |
| R415 | 0603 | 1.5 kΩ |
| C404, C405 | 0603 | 18 pF |
| R413, R417, R420 | 0603 | 220 Ω |

| Designator | Footprint | Comment |
|---|---|---|
| C400 | 0603 | 270 nF |
| R408, R411 | 0603 | 39 kΩ |
| C411, C419 | 0603 | 47 nF |
| JP401 | 2-557101-5 | 100PIN_T&MT |
| C401, C403, C407 | CASE B | 4.7 µF |
| C420 | CASE D | 100 µF |
| Q400 | Crystal | 19.2 MHz |
| SW400 | DC JACK | DC JACK |
| C409, C413, C415, C417 | ECASE-B | 10 µF |
| IC400 | HVQFN32-SMT | ISP1504x1 |
| U1, U2 | IP4359CX4/LF | IP4359CX4/LF |
| S400, S401, S402, S403, S404, S405, S406, S407, S408, S409, S410, S411, S412 | SIP2-S | SIP2-S |
| JP400, JP402, JP403 | SIP3 | Header 1 x 3 |
| IC401 | SO-8 | NDS9435A |
| IC404 | TSSO5X6-G16 | MAX8869 |
| IC405 | TSSO5X6-G16 | MAX8869EUE33 |
| IC406 | TSS05x6-G14/X.3 | SN74LV14PWLE |
| IC407 | SOP_8 | MIC2026 |
| CON400 | USB_A | USB CON TYPE A |
| CON402 | USB_AB | USB mini-AB receptacle |
| CON401 | USB_B | USB CON TYPE B |
| POT101 | VARR | 100 kΩ |
| D400, D401 | 3MM_LED | LED3 |

# 9. Abbreviations

**Table 6. Abbreviations**

| Acronym | Description |
|---|---|
| ASIC | Application-Specific Integrated Circuit |
| ESD | ElectroStatic Discharge |
| ESR | Effective Series Resistance |
| FPGA | Field Programmable Gate Array |

| Acronym | Description |
|---|---|
| OTG | On-The-Go |
| PCB | Printed Circuit Board |
| T&MT | Transceiver and Macrocell Tester |
| TXCMD | Transmit Command |
| ULPI | UTMI+ Low Pin Interface |
| USB | Universal Serial Bus |
| UTMI | USB 2.0 Transceiver Macrocell Interface |

## 10. References


- Universal Serial Bus Specification Rev. 2.0
- On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3
- ISP1504A1; ISP1504C1 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet
- UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1
- USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2

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